a conducting signal path, said conducting signal path being electrically connected to said conducting interface, said conducting interface being electrically connected to said input receiver, said signal path carrying said digital signal thereover; and

wherein said conducting interface is substantially rectangular in planar view and said conducting signal path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of said conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 13 (new). The apparatus according to Claim 12, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 14 (new). The apparatus according to Claim 13, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of the said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

Claim 15 (new). The apparatus according to Claim 14, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 16 (new). The apparatus according to Claim 13, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 17 (new). The apparatus according to Claim 16, further comprising a circuit substrate, wherein said input receiver and said conducting interface are located on said circuit substrate.

Claim 18 (new). The apparatus according to Claim 17, wherein said circuit substrate comprises a printed circuit board and wherein said conducting interface is a pad and said conducting signal path is a trace.

Claim 19 (new). The apparatus according to Claim 18, wherein said pad is substantially square in planar view.

Claim 20 (new). The apparatus according to Claim 18, wherein said trace has a width which is 1/5th of a width of said pad to which said trace is connected.

Claim 21 (new). The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of said pad to which said trace is connected.

Claim 22 (new). The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said pad has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said trace has a width of 4 mils and a thickness of 1.2 mils.

Cont A4

Claim 23 (new). The apparatus according to Claim 18, wherein the apparatus is a memory system which further comprises a memory device, wherein said signal source is a memory controller which generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

Claim 24 (new). The apparatus according to Claim 23, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

Claim 25 (new). The circuit substrate for a signal-triggered digital circuit, said circuit substrate comprising:

a conducting interface, substantially rectangular in planar view, for electrical connection to an input receiver, said input receiver receiving a digital signal over said digital circuit and being responsive to triggering induced by said digital signal;

a conducting signal path having a width which is 1/5th of a width of said conducting interface, said conducting signal path being connected to said conducting interface, said signal path carrying said digital signal thereover; and

wherein said conducting path connected to said conducting interface has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which said path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 26 (new). The circuit substrate according to Claim 25, wherein said conducting interface is substantially square in planar view.

Claim 27 (new). The circuit substrate according to Claim 25, wherein said conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which said conducting signal path is connected.

Claim 28 (new). The circuit substrate according to Claim 25, wherein when said input receiver is mounted to said conducting interface, said conducting interface has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said conducting signal path has a width of 4 mils and a thickness of 1.2 mils.

Claim 29 (new). The circuit substrate according to Claim 25, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 30 (new). The circuit substrate according to Claim 29, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital

signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

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Claim 31 (new). The circuit substrate according to Claim 30, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 32 (new). The circuit substrate according to Claim 29, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 33 (new). The circuit substrate according to Claim 32, wherein said circuit substrate comprises a printed circuit board, said conducting interface is a pad and said conducting signal path is a trace.

Claim 34 (new). The circuit substrate according to Claim 33, said circuit substrate further comprising an input receiver and a signal source for generating said digital signal.

Claim 35 (new). The circuit substrate according to claim 34, said circuit substrate further comprising a memory device, wherein said signal source is a memory controller which generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

Claim 36 (new). The circuit substrate according to Claim 35, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

IN THE DRAWINGS:

It is requested that the two sheets of drawings containing Figures 7 and 8 be cancelled and replaced with the enclosed substitute sheets, for which duplicates have been submitted to show the proposed drawing changes in red. Three additional sheets have been provided for Figures 1A, 1B, and 1C, respectively.

REMARKS

Applicants have amended the specification and claims in order to comply with the Examiner's objections as set out in the Office Action dated June 19, 2000 in parent application serial no. 08/951,556.

The specification of the present continuation application reflects the language of the parent application, as originally filed, together with all amendments of record thereto which had not been objected to by the Examiner.

Figure 1A has been added. It shows a schematic diagram of the prior art. This is a diagram of a component 7 with multiple leads 5 on a printed circuit board 14. It shows a component 7 with multiple leads 5 connected to a pad 12 on the printed circuit board 14 as